LISTING OF CLAIMS IN THE CASE

Please amend Claims 1, 8, 11, 14, and 21, as follows.

1. (Currently Amended) A computer implemented method of generating an order of loading data into a programmable device comprising the steps of:

a) identifying a plurality of memory cells in a hierarchical schematic representation of an architecture of a programmable device for which a programming order is desired;

b) automatically determining a plurality of addresses corresponding to said plurality of memory cells;

c) automatically determining a plurality of logical names for said plurality of memory cells; and

d) based on an order in which said plurality of addresses are to be loaded into said programmable device, automatically storing said plurality of logical names for said plurality of memory cells within a data structure within computer readable memory, wherein said data structure describes an order in which to program said programmable device.

2. (Original) The method of Claim 1 wherein step a) comprises the step of:

a1) identifying said plurality of memory cells which are at the lowest level in said schematic hierarchy.

3. (Original) The method of Claim 1 wherein step b) comprises the steps of:

b1) determining a wordline associated with one memory cell of said plurality of memory cells; and

b2) determining a bitline associated with said one memory cell of said plurality of memory cells.

4. (Original) The method of Claim 1 further comprising the step of:

e) repeating said steps a) through d) for each configuration block of said programmable device.

5. (Previously Amended) The method of Claim 1 wherein said d) comprises:

determining whether there is a configuration bit at an address of said plurality of addresses in a configuration block.

6. (Previously Amended) The method of Claim 5 wherein said d) further comprises:

placing a spacer in said data structure of said plurality of logical names in responsive to a determination that there was no configuration bit at said address in said configuration block.

7. (Original) The method of Claim 1 wherein said programmable device is a complex programmable logic device (CPLD).

8. (Currently Amended) A computer implemented method of generating an order of loading data into a programmable logic device comprising the steps of:

a) accessing a data structure comprising a plurality of logical names corresponding to a plurality of addresses in a hierarchical schematic representation of an architecture of a programmable logic device;

b) accessing a data structure specifying an order in which said plurality of addresses are to be loaded into said programmable logic device;

c) automatically ordering said plurality of logical names from step a) based on the order specified in said data structure in step b); and

d) automatically storing said ordered plurality of logical names from step c) in a data structure within computer readable memory, wherein said ordered plurality of logical names describe an order of loading data into said programmable logic device.

9. (Original) The method of Claim 8 further comprising the step of:

e) storing a placeholder in said data structure of said plurality of logical names from step d).

10. (Original) The method of Claim 8 further comprising the step of:

e) determining whether there is a configuration bit at one address of said plurality of addresses.

11. (Currently Amended) The method of Claim 8 wherein step a) further comprises the steps of:

a1) identifying a plurality of memory cells in said hierarchical schematic representation of said architecture of said programmable device;

a2) identifying said plurality of addresses corresponding to said plurality of memory cells; and

a3) determining said plurality of logical names for said plurality of memory cells.

12. (Original) The method of Claim 11 wherein said plurality of memory cells are configuration bits.

13. (Original) The method of Claim 11 wherein step a) comprises the step of:

a) identifying said plurality of memory cells which are at the lowest level in said schematic hierarchy.

14. (Currently Amended) A system comprising a processor coupled to a bus and memory coupled to said bus wherein said memory contains processor instructions for implementing a method of generating an order of loading data into a programmable logic device, said method comprising the steps of:

a) identifying a plurality of memory cells in a hierarchical schematic representation of an architecture of a programmable device for which a programming order is desired;

b) automatically determining a plurality of addresses corresponding to said plurality of memory cells;

c) automatically determining a plurality of logical names for said plurality of memory cells; and

d) based on an order in which said plurality of addresses are to be loaded into said programmable logic device, automatically storing said plurality of logical names for said plurality of memory cells within a data structure within computer readable memory.

15. (Original) The method of Claim 14 wherein step a) comprises the step of:

a1) identifying said plurality of memory cells which are at the lowest level in said schematic hierarchy.

16. (Original) The method of Claim 14 wherein step b) comprises the steps of:

b1) determining a wordline associated with one memory cell of said plurality of memory cells; and

b2) determining a bitline associated with said one memory cell of said plurality of memory cells.

17. (Previously Amended) The method of Claim 14 wherein said d) comprises:

determining whether there is a configuration bit at an address of said plurality of addresses in a configuration block.

18. (Previously Amended) The method of Claim 17 wherein said d) further comprises:

placing a spacer in said data structure of said plurality of logical names responsive to a determination that there was no configuration bit at said address in said configuration block.

19. (Original) The method of Claim 14 wherein said programmable device is a complex programmable logic device (CPLD).

20. (Original) The method of Claim 14 further comprising the step of:

e) repeating said steps a) through d) for each configuration block of said programmable logic device.

21. (Currently Amended) The computer implemented method of Claim 1, further comprising:

e) receiving a modification to said hierarchical schematic representation of said architecture of said programmable device; and

f) repeating said a) through d) using said modified hierarchical schematic representation of said architecture of said programmable device to automatically generate a new order in which to program said programmable device.